includes a system LSI cell portion which in turn includes a plurality of functional blocks for realizing specific functions. Each of the functional blocks serves as a unit circuit and is arranged on a semiconductor chip. As further described in the last full paragraph on page 6 in connection with Figures 2A and 2B, the system LSI cell portion 7 is composed of a silicon chip 1, and the functional blocks 2 to 6 formed on the surface of silicon chip 1. As is evident from these passages, the invention comprises a silicon chip divided into distinct, functional blocks.

Part of the significance of such arrangements, particularly in connection with the use of an LSI cell portion as described in connection with the similarly disclosed and recited global wiring layer, is the electrical interconnection characteristics described on page 9 of the specification. As described therein in connection with the illustration of Figure 4B, the silicon chip 1 is formed to create functional blocks 2 to 6. As a consequence of such formation, the respective gates in the functional blocks are connected to each other by the use of a wiring pattern that is part of the LSI wiring layer. Afterward, external terminals are formed to contact between their respective functional blocks 2 to 6 utilizing pads 2a to 6a. The global wiring layer provides the interconnection between such pads, and hence provides the electrical interconnection between gates from different functional blocks.

As is evident from these and other passages in the present application, the present invention provides a structure comprising a silicon chip divided into a plurality of functional blocks, each of the functional blocks having a plurality of gates, with electrical interconnection among gates inside a single one of the functional blocks provided by wiring in a silicon chip. Subsequently attached to the silicon chip is a global wiring layer, which provides electrical interconnection between respective functional blocks. Therefore, electrical interconnection within a given functional block is provided by wiring within the silicon chip, whereas electrical interconnection between respective functional blocks is provided by the global wiring layer.

The applied SAITOU et al. reference describes a method and apparatus of fabricating an electric circuit pattern on a thick and thin film hybrid multilayer wiring substrate. Throughout such reference, element 30 is described as an LSI, without any indication whatsoever of features relating to the functional blocks and the gates disposed therein, or the intra-functional block or inter-functional block electrical connections described in the present application and recited in the amended claims.

In summary, the present invention as disclosed and claimed describes an arrangement in which the respective functional blocks are connected to each other by the use of the

global wiring layer. In contrast, the SAITOU reference does not disclose such global wiring layer.

The Office action suggests that the element identified by reference numeral 20 in Figure 13 of the applied reference corresponds to the global wiring layer. However, applicants respectfully suggest that such construction is incorrect, as element 20 represents the wiring layer for connecting the external terminals of the LSI chip 30 with the wiring portion 10 on the substrate. As a result, it does not indicate the wiring layer for mutually connecting the functional blocks on the LSI chip.

As the applied reference fails to disclose the entirety of that which is recited in the present claims, applicants respectfully suggest that the present anticipation rejection cannot be maintained.

In light of the amendments described above and the arguments offered in support thereof, applicants believe that the present application is in condition for allowance and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may contact the undersigned attorney so that this application may continue to be expeditiously advanced.

Attached hereto is a marked-up version of the changes made to the claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

--1. (twice amended) A system semiconductor device, comprising:

a system LSI cell portion [which includes] comprising a semiconductor chip divided into a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip, each of the functional blocks comprising a plurality of gates; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

wherein:

the global wiring layer comprises:

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer; and

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring

within the system LSI cell portion, and electrical interconnection between gates of different said the functional blocks is provided by the global wiring layer.--

Claim 6 has been amended as follows:

--6. (twice amended) A system semiconductor device, comprising:

a system LSI cell portion [which includes] comprising a semiconductor chip divided into a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip, each of the functional blocks comprising a plurality of gates; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;[,]

wherein[:] the global wiring layer comprises[;]:

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer; and

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring within the system LSI cell portion, and electrical

interconnection between gates of different said the functional blocks is provided by the global wiring layer.--

Claim 12 has been amended as follows:

--12. (twice amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which are constructed to serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer separate from the fabricated system LSI cell portion by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the separately fabricated global wiring layer such that [the] electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer.--

Claim 16 has been amended as follows:

--16. (twice amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that [the] electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, a second wiring layer, an insulating layer, and inner bumps on the semiconductor substrate.--

Claim 17 has been amended as follows:

--17. (amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a

plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that [the] electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.--

a system LSI cell portion comprising a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring within the system LSI cell portion, and electrical interconnection between gates of different said functional blocks is provided by the global wiring layer.--

Please charge the fee of $84 for the extra independent claim added herewith, to Deposit Account No. 25-0120.

REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1, 2, 6, 7, and 9-23 under 35 USC §102(b) as being anticipated by SAITOU et al. 5,162,240. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

As noted throughout the present application, including the paragraph beginning on page 3, line 13, the invention